The digital data input may turn on or off switches and may control a quantity of switched capacitors, to provide the digital-to-analog conversion.

[0019] In some example embodiments, RF DAC **110** may also be coupled to a multiphase clock generator **112**. The multiphase clock generator **112** may generate two sampling clocks ϕ_P **116**A and ϕ_N **116**B, both of which serve as an input to RF DAC **110**. These sampling clocks are used by RF DAC **110** to sample incoming digital data/digits **105** with a sampling period, T (for example, of $T=1/f_C$) **198** and convert the sampled digits into the voltage domain to generate an analog output **140**.

[0020] In some example embodiments, tuning a time delay between sampling clocks ϕ_P **116**A and ϕ_N **116**B may vary an impulse response and, as a consequence, an amplitude of the analog output **140** of the RF DAC **110**. The tuning of the sampling clocks ϕ_P **116**A and ϕ_N **116**B may be performed via a control signal **195**. Therefore, rather than employ two sampling clocks having a constant 180 degree phase shift, multiphase clock generator **112** may, in some example embodiments, tune the time delay/phase difference between the sampling clocks ϕ_P **116**A and ϕ_N **116**B to vary the gain of the output **140** of RF DAC **110**.

[0021] In some example embodiments, the multiphase clock generator **112** may include a delay-locked loop configured to provide a plurality of different sampling clocks. When this is the case, multiphase-clock generator **112** may select two sampling clocks from the plurality of different sampling clocks to serve as the variable/tunable sampling clocks **116**A-B (labeled ϕ_P and ϕ_N) input to multiphase clock generator **112** to control a desired gain provided by RF DAC **110**. The tuning of the sampling clocks **116**A-B may vary time delay **199** (labeled Δt, or phase difference, $\Delta\theta=2\pi f_c\Delta t$) of the sampling clocks **116**A-B ϕ_P and ϕ_N to produce a certain impulse response for the output signal **140**.

[0022] In some example embodiments, tuning multiphase clock generator **112** may, as noted, allow gain/power control of the analog output **140** of RF DAC **110**. By providing gain control at the RF DAC **110**, the front-end of system **100** may, in some example embodiments, not need a separate attenuator at the output of RF DAC **110** to control the gain (for example, power, level, and the like) of analog output **140**. This elimination of the attenuator may, in some example embodiments, improve power efficiency, especially at, for example, low transmit powers.

[0023] Although some of the examples described herein refer to tuning a time delay, Δt between sampling clocks ϕ_P **116**A and ϕ_N **116**B, varying time delay also varies the phase difference ($\Delta\theta$) as well.

[0024] FIG. **2**A depicts an illustrative example of an impulse response $h_{P\text{-}N}(t)$ **205** for the output signal **140** of voltage-mode RF DAC **110**. In the example of FIG. **2**A, sampling clocks ϕ_P **116**A and ϕ_N **116**B have about a fifty percent (50%) duty-cycle, and have a period T, which may be the inverse of the carrier frequency, fc (for example, $T=1/f_C$), although other duty cycles may be used as well. In the example of FIG. **2**A, $h_P(t)$ **211** and $h_N(t)$ **208** represent the impulse responses due to ϕ_P **116**A and ϕ_N **116**B, respectively. Moreover, the amplitude, A, of the impulse responses may be a constant magnitude corresponding to a digital word being converted by the RF DAC **110**.

[0025] FIG. **2**B shows a phase plot of ϕ_P **291** and ϕ_N **292** as well as the corresponding resultant **293** representative of output signal **140**. FIG. **2**B shows that the frequency response of $h_{P\text{-}N}(t)$ **205** may be directly proportional to the following equation:

$$2A*\sin(\Delta\theta/2)=2A*\sin(\pi f_c\Delta t) \quad \text{Equation (1),}$$

wherein Δt represents the time delay between ϕ_P and ϕ_N, ($\Delta\theta$) represents the phase difference delay between ϕ_P and ϕ_N, A represents the magnitude corresponding to a digital word being converted by RF DAC **110**, and sin represents the sine function. As such, the gain of the output signal **140** of voltage-mode RF DAC **110** may be precisely tuned within a wide control range by varying the time delay Δt, which in this example may be controlled over the range of $1/\sin(\pi f_C\Delta t)$ by varying Δt.

[0026] FIG. **2**B shows that as time delay/phase delay ($\Delta t/\Delta\theta$) **199** becomes smaller, the sampling clocks ϕ_P **291** and ϕ_N **292** may cancel each other out most of the time and thus deliver substantially no voltage signals at output **140**, which may maintain relatively high efficiency even at low power levels.

[0027] Referring again to FIG. **2**A, impulse response $h_{P\text{-}N}(t)$ **205** may also show that gain control provides pulse width power control but also offers a control range without the need for extremely narrow pulse generation. Although FIG. **2** depicts impulse responses corresponding to a square wave, this is merely an illustrate example as other types of responses may be achieved as well.

[0028] FIG. **3**A depicts another example system **300** including an example of a voltage-mode RF DAC **110**, in accordance with some example embodiments. System **300** is similar to system **100** in some respects but includes example implementations for the RF DAC **110** and the multiphase clock generator **112**. Moreover, system **300** may be used to provide, in some example implementations, an 8-bit, 2.5-Gigasample per second RF DAC, which has an output gain that can be varied based on time delay as disclosed herein, although other types of RF DACs may be implemented as well.

[0029] RF DAC **110** may include two voltage-mode DACs (labeled "sub DAC). The sub DACs have delayed impulse responses as shown for example at FIGS. **2**A-**2**B. RF DAC **110** may deliver voltage outputs to antenna load R_L **395** via a serial inductance-capacitance (L-C) resonant network **390**, which may include a transformer (labeled L**1** and L**2**) and two capacitors (labeled C and C) intrinsic to each sub DAC.

[0030] In some example embodiments, multiphase clock generator **112** may include delay-locked loop (DLL) **370**. The delay-locked loop **370** may further include a plurality of delay cells **372**A-X to generate a plurality of time delay steps ϕ_0 through ϕ_X. These time delay steps ϕ_0-ϕ_X may be selected by a phase selector **374** under the control of control lines **195** providing ϕ_P **116**A and ϕ_N **116**B. For example, depending on the desired time delay Δt and corresponding gain desired at the output of RF DAC **110**, control lines **195** may select two of the time delay steps ϕ_0-ϕ_X in order to provide sampling clocks ϕ_P **116**A and ϕ_N **116**B. This selection from the plurality of delay cells **372**A-X may be used to vary the time/phase difference between the sampling clocks ϕ_P **116**A and ϕ_N **116**B, which varies the gain at the output of voltage-mode RF DAC **110**. Moreover, this gain control may be relatively immune to integrated circuit technology process, voltage, and/or temperature variations. In some example embodiments, the use of a plurality of delay cells **372**A-X providing a plurality of clocks may provide relatively well-defined and